3E1147

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B. Tech. III - Sem. (Main) Exam., Dec. - 2018

PCC Electronics & Communication Engineering

3EC4 – 04 Digital System Design

EC, EI

Time: 3 Hours **Maximum Marks: 120**

Instructions to Candidates:

Attempt all ten questions from Part A, selecting five questions from Part B and four questions from Part C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used /calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL

2. NIL

PART – A

(Answer should be given up to 25 words only) **[10×2=20]**

All questions are compulsory

Q.1 Write Decimal no. $(125)_{10}$ in BCD. [2]

Q.2 Convert $y = AB + \overline{A}\,\overline{B}$ (sop) form in equivalent POS form. [2]

Q.3 Define Fan-out of logic system. [2]

Q.4 Write the name of two modeling style in VHDL. [2]

Q.5 Draw the state diagram of any one finite state machine (FSM). [2]

Q.6 Find the total no. of select line, when a 8×1 Mux is implemented using 2×1 Mux. [2]

Q.7 Draw the circuit diagram of any two Dynamic memory cell. [2]

Q.8 Write any one use of tristate logic. [2]

Q.9 Write the name of one Parallel Adder. [2]

Q.10 Write VHDL code for $y = A\overline{B}$ in structural model. [2]

PART – B

(Analytical/Problem solving questions) **[5×8=40]**

Attempt any five questions

Q.1 Derive a minimum cost circuit that implement the function- [8]

$$f(x_1 \ldots x_u) = \sum m(4,7,8,11) + D(12,15)$$

Q.2 Draw the output waveform of a four bit serial in parallel out shift register for six clocks. Assume the Data input is =10111011... [8]

Q.3 Implement y= A + BC in ECL logic and explain its working. [8]

Q.4 How SR FF is converted to JK FF? Draw its circuit diagram and explain. How the JK FF determine output when both J = K = 1? [8]

Q.5 Write VHDL code for a Half Adder in Data flow style. [8]

Q.6 How Mux is used for implement combinational logic? Implement y = A+BCD using a Mux. http://www.rtuonline.com [8]

Q.7 Draw the general diagram of a single bit serial Adder. Calculate the total delay taken in Addition of two four bit data in it. [8]

PART – C

(Descriptive/Analytical/Problem Solving/Design Question) **[4×15=60]**

Attempt any four questions

Q.1 Draw the 2 input NAND gate using TTL logic and calculate its minimum noise level at input that disturb the true output for A = B = 0. Assume the supply is V_{DD} = 9 volt. [15]

Q.2 The state diagram of a FSM is given below, design its logic (fig-2(c)) [15]

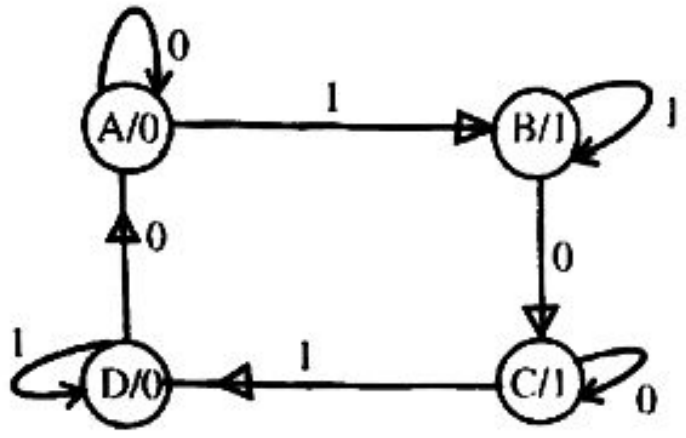

fig - 2(c)

Show its state table, state assignment table and final implemented logic.

Q.3 Draw the state diagram for the logic circuit shown in fig 3(c). [15]

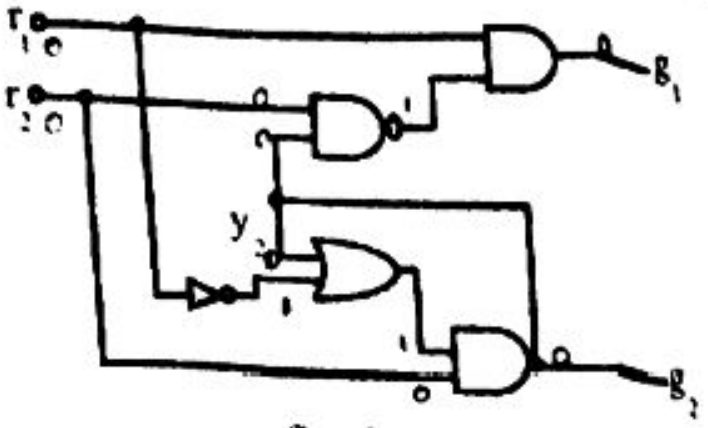

fig - 3(c)

Q.4 Design a 4 bit synchronous down counter using D-FF. Draw its state diagram and all design tables. [15]

Q.5 How FPGA are used for logic implement? Show the OR and AND Space for a 2 variable input. Also show the connection in FPGA for implement $y = \bar{A}\,\bar{B}$ in it. [15]
