3E1150
B. Tech. III - Sem. (Main) Exam., Dec. - 2018
PCC Electronics & Communication Engineering
3EC4 – 07 Electronics Devices
EC, EI

Time: 3 Hours

Maximum Marks: 160

Instructions to Candidates:

Attempt all ten questions from Part A, five questions out of seven questions from Part B and four questions out of five from Part C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used /calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL

[Answer should be .... up to 25 words only]   [10×3=30]

All questions are compulsory

Q.1 Show Bandgap order of GaAs. GaP and SiC in increasing order.

Q.2 Write one difference between Degenerate and non-degenerate semiconductors.

Q.3 Draw Energy band diagram of a semiconductor in thermal equilibrium condition when it's doping level is shown in fig. 3(A)

$N_A = 10^{16}$ cm^{-3}	$N_D = 10^{13}$ cm^{-3}
(Si)	(Si)

fig – 3 (A)

Q.4 Draw characteristic curve of photo diode and solar cell.

Q.5 How many steps are included in one mask during IC fabrication?

Q.6 Write continuity equation under thermal equilibrium conduction and open circuit condition but exposed with photon.

Q.7 Write one difference between LED and LASER diode.

Q.8 Show diode static and dynamic resistance on its I-V characteristic.

Q.9 Define sheet resistance and write its unit.

Q.10 Write the name of two recombination center in a lattice.

PART – B

(Analytical/Problem solving questions)   [5×10=50]

Attempt any five questions

Q.1 Calculate the contact Potential between point 1 & 2 in a semiconductor, shown in fig 1(B) at room temperature.
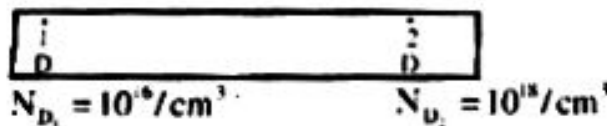

$N_{D_1} = 10^{6}/cm^3$ $N_{D_2} = 10^{18}/cm^3$

fig – 1(B)

Assume $ni = 1.5 \times 10^{10}/cm^3$

Q.2 How Zener diode is used for voltage regulation. Design such regulator in which input voltage vary in (10 – 12) volt and across load we need constant 6 volt, even the load is changed between 10 – 12 kΩ range.

Q.3 Draw input and O/P characteristics of common base (CB) configuration and show all h – parameter on it.

Q.4 Define the following fabrication process:

(i)   Oxidation and

(ii) Ion implementation

Q.5 In NPN transistor the concentration of electron in base region change as shown in fig 5 (B).
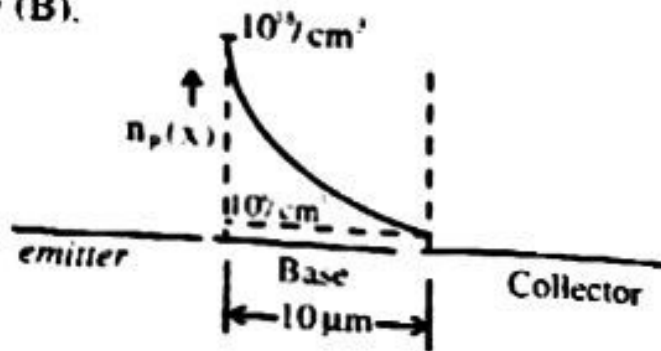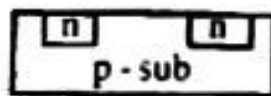

fig. – 5 B

Then calculate the diffusion current density in base region. Assume the mobility constant of electron is $fe_n = 1400 \frac{cm^2-volt}{sec}$ at room – temperature.

Q.6 Draw MOSFET VI characteristic at different gate – source (V_{GS}) voltage and show the atomic and saturation region on it.

Q.7 Show all fabrication step to achieve following structure:

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PART – C

**(Descriptive/Analytical/Problem Solving/Design Question)** [4×20=80]

Attempt any four questions

Q.1 How compound semiconductor are superior than element semiconductor?

Design a $Ga_{1-x}As_x$ semiconductor whose sensitivity is maximum for a photon in infrared region when it is used as photodiode.

Q.2 Draw characteristic of a solar cell and define open circuit voltage and short circuit current on it. How solar cell is used in solar panel for increase in current and voltage rating?

Q.3 Draw the current in following diode circuit (fig. 3C) for the given voltage. Also define storage time. reverse recovery time on it.
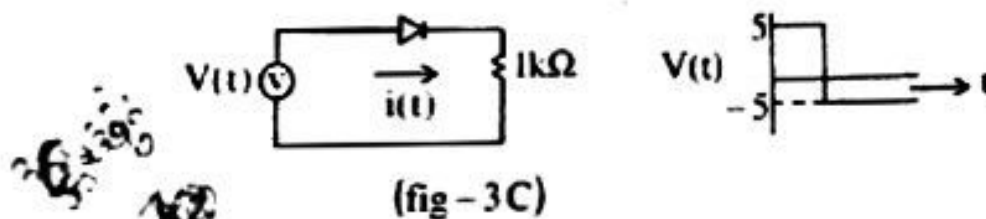
(fig – 3C)

Q.4 Develop small signal MOSFET Model and draw its electrical equivalent circuit & define all model parameters.

Q.5 Write the use of the following:

    (i)   Schottky diode in TTL.

    (ii)   Etching process in IC fabrication

    (iii) Direct bandgap material in LED