3E1150

B. Tech. III - Sem. (Main /Back) Exam., Dec. 2019
PCC Electronics & Communication Engineering
3EC4-07 Electronics Devices
EC, EI

Time: 3 Hours

Maximum Marks: 160

Instructions to Candidates:

Attempt all ten questions from Part A, fiver questions out of seven questions from Part B and four questions out of five from Part C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used /calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL _____

2. NIL _____

PART – A

(Answer should be given up to 25 words only)   [10×3=30]

All questions are compulsory

Q.1 Define Intrinsic and Exterinsic Semiconductor with examples.   [3]

Q.2 How does pure semiconductor behave like a absolute zero temperature and why?   [3]

Q.3 Define drift and diffusion current with equation of net hole current.   [3]

Q.4 Explain role of depletion layer in semiconductor diode with knee voltage.   [3]

Q.5 Give the differences between Silicon [Si] and Gallium Arsenide [GaAs].   [3]

Q.6 What is avalanche breakdown for P – N Junction diode?   [3]

Q.7 Explain working of transistor as a switch. [3]

Q.8 Define stability factor (s) for a transistor. [3]

Q.9 Write the short note on twin – tub fabrication process. [3]

Q.10 Define the steps of Photolithography process. [3]

PART – B

(Analytical/Problem solving questions) [5×10=50]

Attempt any four questions

Q.1 (a) A sample of Si at a given temperature "T" in intrinsic condition has a resistivity of $25 \times 10^4 \, \Omega$ - cm. The sample is now doped to the extent of 4×10^{10} donor atoms 1 cm^3 and 10^{10} acceptor atom/cm^3, find the total conduction current density if an electric field of 4V/cm is applied across the sample. Given that μ_n=1250 cm^2/V– s, μ_p = 475 cm^2/V – s at the given temperature. [6]

(b) Explain band gap theory for semiconductor materials. [4]

Q.2 (a) Difference between breakdown condition for P–N junction diode and Zener diode. [5]

(b) Derive the relation for continuity equation in P –N Junction. [5]

Q.3 (a) Explain the process P – type and N – type semiconductor formation with doping. [5]

(b) Discuss for C-V characteristics of MOS capacitor. [5]

Q.4 Write the Ebers-Moll equation sketch the circuit model, which satisfies these equations. [10]

Q.5 Write short note on –

(a) . Light Emitting Diode [3]

(b) . Photo diode [3]

(c) . P-V plate [4]

Q.6 (a) . Explain in detail the ion-implantation process. [5]

(b) , Define the steps of fabrication with flow chart for CMOS. [5]

Q.7, Discuss the types of oxidation process involve in CMOS fabrication. [10]

PART – C

(Descriptive/Analytical/Problem Solving/Design Questions) [4×20=80]

Attempt any two questions

Q.1 In reference to semiconductor write short note on –

(a) . Mobility [5]

(b) , Conductivity [5]

(c) . Degenerate and Non – degenerate [10]

Q.2 (a) Explain the motion of Electrons in periodic lattices. [4]

(b) . Differentiate direct and indirect band gap in context of E – R diagram. [12]

(c) : Describe the theory of sheet resistance. [4]

Q.3 (a) . Explain the working of NPN transistor with characteristics. [6]

(b) . Which configuration of transistor is used generally and why? [8]

(c) . Why small signal model analysis used for MOS transistor? [6]

Q.4 (a) Derive relation for P-N Junction's Poisson equation. [6]

(b). Design I-V characteristics for Schottky diode and give application of Zener diode. [8]

(c). Define transconductance for small signal Model of MOS. [6]

Q.5 (a) Explain process of fabrication of CMOS in detail with neat and clean sketch for each step. [10]

(b) Design CMOS circuit for NAND gate. [10]