5E1391

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B.Tech. V- Semester (Main) Examination, Nov. - 2019

ESC Electronics & Comm. Engg.

5EC 3-01 Computer Architecture

Time : 2 Hours

Maximum Marks : 80

Min. Passing Marks : 28

*Instructions to Candidates:*

*Attempt all five questions from Part A, four questions out of six questions from Part B and two questions out of three from Part C.*

*Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly). Units of quantities used/calculated must be stated clearly.*



## PART - A

(Answer should be given up to 25 words only)

All questions are compulsory (5×2=10)

1. What is Von - Neuman Architecture?
2. What do you mean by computer structure?
3. What is virtual memory.
4. Mention the various phases in executing an instruction.
5. Write the rules to perform addition an floating point number.

## PART - B

(Analytical/Problem solving questions)

Attempt any four questions (4×10=40)

1. What is cache memory. How to improve cache performance? Discuss.
2. Explain the pipelining in detail.
3. Explain in detail about the bus Arbitration techniques in DMA.
4. What is the use of DMA controller.
5. What are the addressing modes Explain each in brief with diagram.
6. Explain flynn's classification of parallel processing with necessary diagram.

## PART - C

(Descriptive/Analytical/Problem Solving/Design Question)

Attempt any two questions (2×15=30)

1. Explain various instruction formats and illustrate the same with an example.
2. Explain with an example about the operations and operands of the computer hardware?
3. Explain in detail about the memory technologies?