5E1391

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# 5E1391

## B. Tech. V - Sem. (Main / Back) Exam., January - 2022

## ESC Electronics & Communication Engineering

## 5EC3 – 01 Computer Architecture

**Time: 2 Hours** **Maximum Marks: 80**

**Min. Passing Marks: 28**



*Instructions to Candidates:*

***Attempt all five questions from Part A, four questions out of six questions from Part B and two questions out of three from Part C.***

*Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used /calculated must be stated clearly.*

*Use of following supporting material is permitted during examination. (Mentioned in form No. 205)*

1. NIL 2. NIL

## PART – A

**(Answer should be given up to 25 words only)** **[5×2=10]**

**All questions are compulsory**

Q.1 What is virtual memory?

Q.2 What is meant by an interleaved memory?

Q.3 Define segmentation.

Q.4 Explain input-output processor.

Q.5 Write the rules to perform addition of floating point numbers.

## PART – B

**(Analytical/Problem solving questions)** **[4×10=40]**

**Attempt any four questions**

Q.1 What are the addressing modes? Explain each in brief with diagram.

Q.2 Describe in detail about the bus arbitration techniques in DMA.

Q.3 What are the 3 different cache memory schemes? Explain in detail.

Q.4 What are the various modes of data transfer to and from the computer system? Explain.

Q.5 Explain Flynn's classification with suitable examples:

Q.6 What is the difference between cache memory & associative memory? Explain in detail.

## PART – C

**(Descriptive/Analytical/Problem Solving/Design Questions)** **[2×15=30]**

**Attempt any two questions**

Q.1 Describe different instruction formats and illustrate the same with an example.

Q.2 Describe in detail about the memory technologies.

Q.3 Write short notes on –

(a) DMA controller

(b) Stacks & queues

(c) Arithmetic pipeline

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