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B. TECH. III Sem Main/Back Exam.

2025-2026

Electrical and Electronics Engineering and

Electrical Engineering

(3EX4-04/3EE4-04) - Analog Electronics

Common to EE, EX

Time : 3 Hours]

[Max. Marks : 70

[Min. Passing Marks :

Instructions to Candidates :

Part-A : Short answer questions (up to 25 words) $10 * 2 = 20$ marks.

All ten questions are compulsory.

Part-B : Analytical/Problem Solving questions $5 * 4 = 20$ marks.

Candidates have to answer 5 questions out of 7.

Part-C : Descriptive/Analytical/Problem Solving questions $3 * 10 = 30$ marks.

Candidates have to answer 3 questions out of 5.

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly.

Units of quantities used/calculated must be stated clearly.

Use of following supporting materials is permitted during examination.

(Mentioned in form No. 205)

Part-A

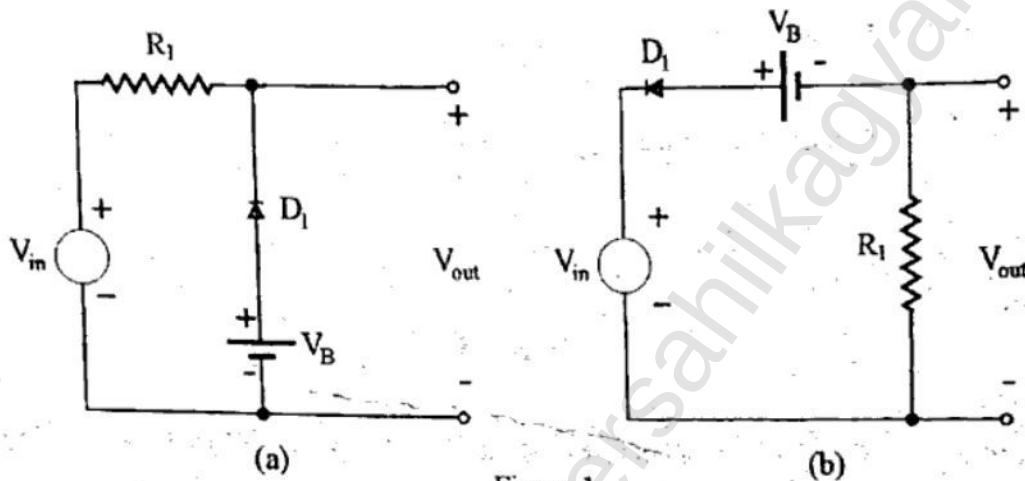
10x2=20

- Q.1 Define Thermal Runaway in Bipolar Junction Transistors. [2]
- Q.2 What is the role of biasing in transistors? [2]
- Q.3 Differentiate between degenerate and non-degenerate semiconductors. [2]
- Q.4 What is the significance of carrier life time? [2]
- Q.5 Sketch the space charge and electric field along a $p+n$ junction diode under equilibrium. [2]
- Q.6 Differentiate between Zener and Avalanche Breakdown. [2]
- Q.7 Differentiate between depletion and enhancement mode operation of MOSFET. [2]
- Q.8 Why does MOS stack act as capacitor? [2]
- Q.9 Define cut-off frequency of amplifier. [2]
- Q.10 Calculate the voltage gain of common base amplifier. [2]

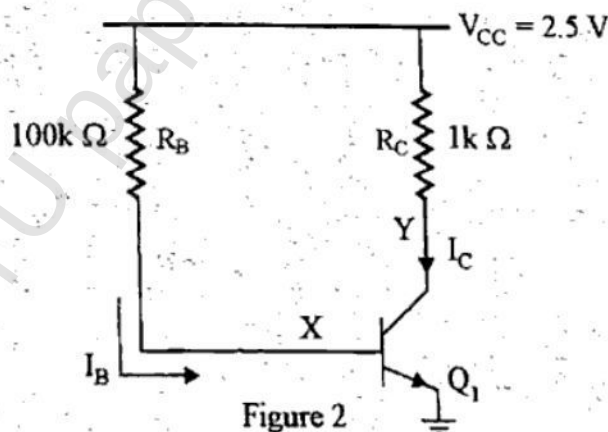
Part-B

5x4=20

- Q.1 If the input is given by $V_{in} = 5 \cos \omega t$, $V_B = 2$ V, analyze and plot the output of each circuit in Fig. 1, as a function of time. Assume an ideal diode model. Also sketch the transfer characteristics for the same. [4]



- Q.2 Determine the dc bias voltage V_{CEQ} and the current I_{CQ} for the circuit shown below in (Fig. 2). Also calculate the stability factor of the circuit if β of transistor is 99. [4]



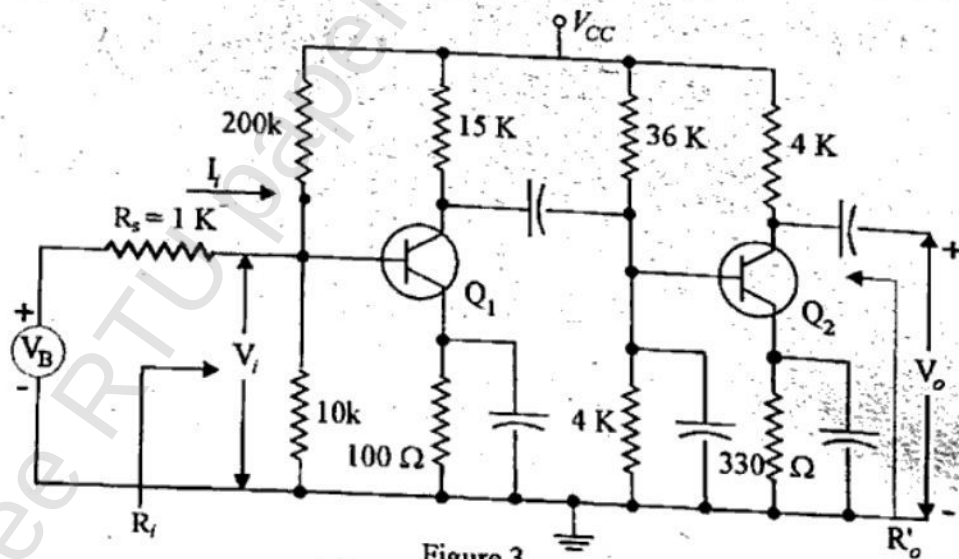
- Q.3 Consider Silicon at $T = 300$ K. contains an acceptor impurity concentration of $N_a = 10^{16} \text{ cm}^{-3}$. Determine the concentration of donor impurity atoms that must be added so that the silicon is n type and the Fermi energy is 0.20 eV below the conduction-band edge. [4]

- Q.4 Derive an expression to establish the dependence of intrinsic carrier concentration on the temperature for a given semiconductor. [4]
- Q.5 Derive the expression to calculate the voltage gain and input resistance for Common Emitter Amplifier with emitter degeneration Resistance R_E . [4]
- Q.6 Explain the Accumulation, Depletion and Inversion mode operation of MOSFET using energy band diagrams. [4]
- Q.7 How Zener diode is used as Voltage? Explain with suitable example. [4]

PART C

3x10=30

- Q.1 Using approximate/simplified small signal model, calculate the voltage gain A_v of the circuit shown in Fig. 3 by considering $\beta = 49$, $I_{CQ} \approx I_{EQ} \approx 1.16$ mA. Also assume both the transistors to be identical and capacitors to be large enough. [10]



Q.2 For an abrupt Silicon, n^+p junction (area = 0.0001 cm^2), we have following parameters at 300 k : [10]

N Side

$N_D = \text{Very High}$

$\tau_p = 10 \mu\text{s}$

$\mu_n = 100 \text{ cm}^2/\text{V-s}$

$\mu_p = 450 \text{ cm}^2/\text{V-s}$

P Side

$N_A = 10^{17} \text{ cm}^{-3}$

$\tau_n = 0.1 \mu\text{s}$

$\mu_n = 700 \text{ cm}^2/\text{V-s}$

$\mu_p = 200 \text{ cm}^2/\text{V-s}$

Calculate the peak electrical field and depletion capacitance for the reverse bias of 100 V. For a certain forward bias, we have current flow of 20 mA in the device, calculate the total excess stored electron charge on the p -side for this bias and electrical field far away from the depletion region in the p -side.

Q.3 Derive the Current-Voltage characteristics of n -type Enhancement MOSFET by considering charge sheet approximation. Also discuss the channel length modulation to explain the behavior in saturation regime. [10]

- Q.4 (a) Design a full-wave rectifier to deliver an average power of 2 W to a cellphone with a voltage of 3.6 V and a ripple of 0.2 V.
(b) Design a clamper to perform following operation (Fig. 4)

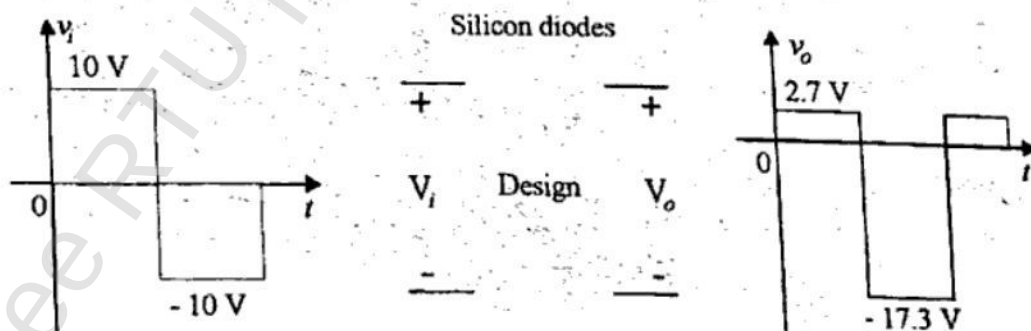


Figure 4

- (c) Sketch v_o and i_R for the circuit shown below in Fig. 5 : [10]

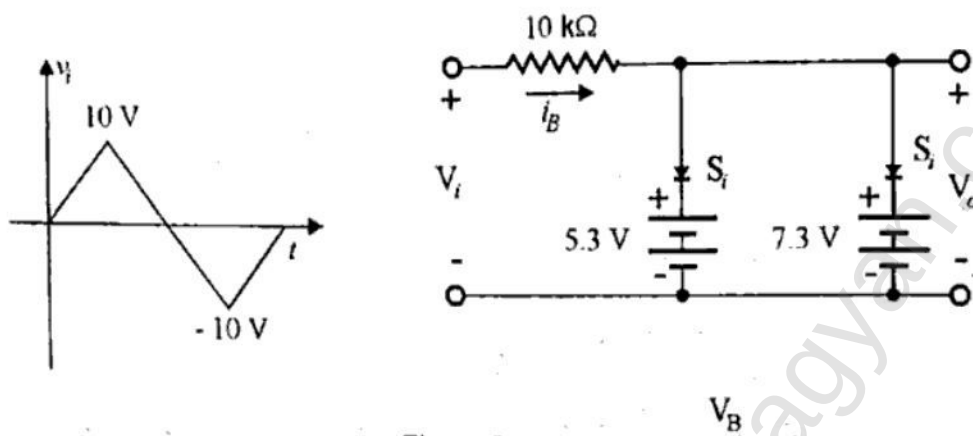


Figure 5

- Q.5 Determine the values of R_C , R_E , R_1 , and R_2 for the network shown in Fig. 6 for the operating points indicated. [10]

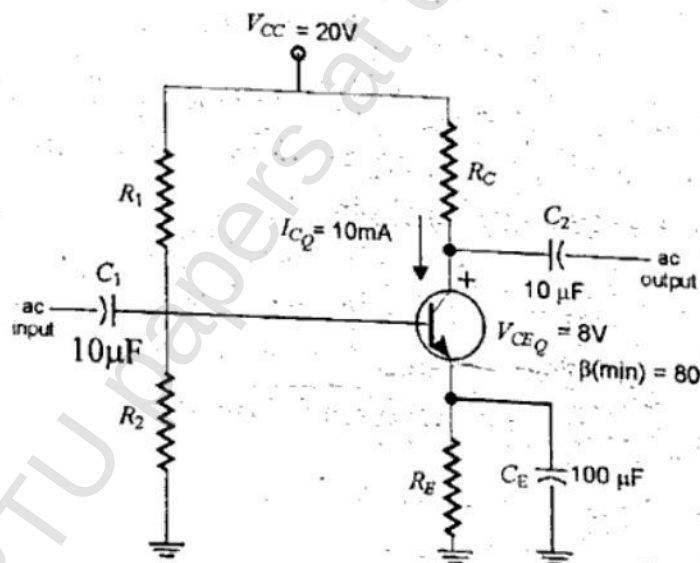


Figure 6
